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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,167	KIM ET AL.	
	Examiner	Art Unit	
	Joey Bednash	2461	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to amendments filed 15 November 2010. Claims 1-12 are pending in the application. Claims 1, 4, 5 and 12 are amended. Claim 13 has been cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Uesugi et al. (US 2002/0114379 A1), hereinafter "Uesugi".

Regarding claim 1, AAPA discloses a demodulation apparatus for receiving signals by an adaptive modulation and coding method, and demodulating the signals, in an OFDMA based packet communication system, comprising:

a QAM demapper **(Fig. 2, QAM Demapper 25)** for performing the QAM demapping process **(Para [10], lines 3-4)** on the received signals by the modulation methods for each of the sub-channels **(Para [7], lines 4-6, DL MAP describes the modulation methods used in the downlink)** and outputting second data which have a number of bits corresponding to the modulation methods for each of the sub-channels,

when the modulation methods for each of the sub-channels are analyzed **(Fig. 2, Buffers 24, Channel Decoder 27 Para [11] symbols are delayed in the buffers 24 until the decoder can analyze the frame prefix and map information which suggests the demapper cannot perform demapping until the DL MAP is analyzed wherein once the DL MAP which describes the modulation method and channel coding method is analyzed, the demapper can now perform the demapping according to the QAM modulation method that has been determined from analyzing the DL MAP in the decoder. It would have been obvious to one of ordinary skill in the art that the claimed second data that was output from the demapper after gaining knowledge of the modulation method that was analyzed in the decoder would have a number of bits corresponding to the modulation method that was gleaned from analyzing the DL MAP in the decoder.)**;

a slot buffer for storing the second data outputted from the QAM demapper for each slot **(Fig. 2, Slot Buffers 26)**; and

a channel decoder **(Fig. 2, Channel Decoder 27)** for decoding the data stored in the slot buffer **(Para [10], lines 13-14)**, analyzing modulation methods for each of the sub-channels transferring the analyzed modulation methods to the QAM demapper **(Para [7], lines 4-6, Para [11]; It would have been obvious to one of ordinary skill in the art at the time of the invention that the modulation method that is described in the DL MAP that is analyzed by the channel decoder would be transferred to the QAM demapper such that the QAM demapper could perform QAM demapping on the received signals because AAPA indicates the symbols must be delayed in**

buffers 24 until the MAP information is analyzed by the channel decoder. This provides the suggestion that the channel decoder would analyze the DL MAP information in order to provide the modulation method information gleaned from the analysis to the QAM demapper such that the demapping could now take place.), reading valid data corresponding the number of bits for the analyzed modulation methods from among the first data and the second data **(Fig. 2, Para [10], the channel decoder decodes the data that has been QAM demapped after it passes "through a slot buffer 26." As discussed above, the data that was demapped according to the QAM modulation would have valid data corresponding to the number of bits for the analyzed modulation methods. While AAPA does not describe the first data, it is examiner's position that reading the second data as suggested by AAPA satisfies the limitation because the terms "from among" does not require the data to be read from the first data)**, reading the second data **(Fig. 2, Para [10], the channel decoder decodes the data that has been QAM demapped after it passes "through a slot buffer 26.")**, demodulating the valid data, and outputting the demodulated data **(Para [10], lines 5-6)**.

AAPA does not disclose performing a QAM (Quadrature Amplitude Modulation) demapping process on the received signals by a modulation method using a maximum modulation ratio, and outputting first data which have a number of bits corresponding to the modulation method using the maximum modulation ratio until modulation methods for each of the sub-channels are analyzed, and storing the first data in the slot buffer.

Uesugi discloses performing a QAM (Quadrature Amplitude Modulation) demapping process on the received signals by a modulation method using a maximum modulation ratio and outputting first data which have a number of bits corresponding to the modulation method using the maximum modulation ratio **(Para [0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern; Figs. 5 and 6, Para [0068]-[0074] teaches demapping 16QAM with a 64QAM demodulation pattern; Figs. 7 and 8, Para [0076]-[0080] teaches demapping QPSK with a 64QAM demodulation pattern; It would have been obvious to one of ordinary skill in the art at the time of the invention that demapping QPSK, 16 QAM, 32 QAM and 64 QAM utilizing a 64 QAM modulation pattern or constellation as taught by Uesugi would result in a number of bits which are represented by 64 QAM symbols)**.

Uesugi teaches that by demapping (i.e. demodulating) received QPSK and 16QAM signals using the 64QAM demodulation pattern (i.e. map) without any knowledge of the modulation scheme applied at the transmitter "it is possible to reduce the time during which a modulation level broadcast signal is demodulated and then data is demodulated like the conventional method, and to decrease data delay" **(Para [0095])**. Para [0095] of Uesugi teaches that received data can be demapped using the maximum modulation ratio (i.e. 64 QAM) without knowledge of the modulation method of the receiver, yet the modulation level broadcast signal (i.e. DL MAP information) is still demodulated such that after the modulation level broadcast signal which carries the information of the modulation method used in the transmission is demodulated, then

data is demodulated like the conventional method. It is examiner's position that this portion of Uesugi suggests performing demapping by the maximum modulation ratio until the modulation scheme which is used in the transmission is determined from the modulation level broadcast signal, and then data is demodulated the conventional way by using the constellation which corresponds to the modulation scheme used in the transmission.

It would have been obvious to one of ordinary skill in the art at the time of the invention to perform demapping using the maximum modulation ratio until the DL MAP information was analyzed and to store the first data that resulted from the demapping in the slot buffers until the DL MAP was analyzed to determine the modulation method used in the transmission of data because the teaching can found in AAPA that data must be delayed in buffers 24 until the DL MAP is analyzed, and Uesugi suggests that delay can be decreased by using the maximum modulation ratio until the modulation level broadcast signal is demodulated.

Regarding claim 4, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the slot buffer comprises:

a first slot buffer for storing the first data outputted from the QAM demapper until the modulation methods for each of the sub-channels of the received signals are analyzed by the channel decoder **(AAPA: Fig. 2, Slot Buffers 26, it would be obvious that the symbols demapped as taught by Uesugi could be stored in the Slot buffer of Fig. 2)**; and

a second slot buffer for storing the second data outputted from the QAM demapper, once the modulation methods for each of the sub-channels of the received signals are analyzed by the channel decoder **(AAPA: Fig. 2, Slot Buffers 26, (Fig. 2, Slot Buffers 26; Para [10], Para [11], Para [13])**.

Regarding claim 5, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 4. It would have been merely a matter of obvious engineering design choice with respect to in which slot buffer illustrated in Fig. 2 of AAPA the demapped data is stored. Storing data demapped by the methods taught by Uesugi in one slot buffer and the data demapped by the conventional methods as taught by AAPA in a different slot buffer would not produce a new and unexpected result.

Regarding claim 6, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the channel decoder reads the MAP information in the former part of a frame among the symbol data stored in the slot buffer, and analyzes the modulation methods for each of the sub-channels **(AAPA, Figs. 1-3, Para [10]-[11]; The Channel decoder 27 decodes data that passes through the slot buffers, and the MAP info is in the former part of the frame.)**.

Regarding claim 7, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the QAM demapper performs a demapping process on the received signals by the modulation methods for each of the sub-channels, and stores the output data in the slot

buffer, once the modulation methods for each of the sub-channels are analyzed by the channel decoder **(AAPA, Para [10], [11], [13])**.

Regarding claim 8, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case data are demodulated by the modulation method using the maximum modulation ratio, a constellation for part of the data is identical with a constellation for the data demodulated by the modulation methods for each sub-channels **(Uesugi: Para [0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern)**.

Regarding claim 9, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 8, wherein the demodulation apparatus further comprises:

an FFT (Fast Fourier Transform) unit for performing FFT on the received signals and outputting the signals **(AAPA; Fig. 2, FFT unit 21; Para [10])**;

a re-ordering buffer for re-ordering the signals outputted from the unit and storing the signals **(AAPA; Fig. 2, Reordering Buffers 22; Para [10])**;

an equalizer for estimating channels using the signals stored in the re-ordering buffer and performing equalization of the signals, and outputting the signals to the QAM demapper **(AAPA; Fig. 2, Equalizer 23; Para [10])**.

Regarding claim 10, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case the modulation method using the maximum modulation ratio is 64QAM, and a

data unit for storing in the slot buffer is 6 bits of data **(Uesugi: Fig. 3)**; the valid data by the 16 QAM modulation method are former 4 bits of data from among the 6 bits of data **(Uesugi: Fig. 5, Para [0074])**.

Regarding claim 11, Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case the modulation method using the maximum modulation ratio is 64 QAM, and a data unit for storing in the slot buffer is 6 bits of data **(Uesugi: Fig. 3)**, the valid data by the QPSK modulation method are 2 bits of data in front of the 6 bits of data **(Uesugi: Fig. 5, Para [0080])**.

Regarding claim 12, the claim is directed towards the method performed by the apparatus of claim 1 and is therefore rejected on the same grounds presented above for claim 1.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Uesugi, further in view of Matsumoto et al. (US 2002/0136207 A1), hereinafter "Matsumoto".

Regarding claim 2, the modification of AAPA with Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)**.

The combination of AAPA and Uesugi does not disclose controlling read enable signals for controlling the data output stored in the slot buffer.

Matsumoto teaches the use of read enable signals for accessing data from a buffer which is activated when a determination is made that the buffer contains valid data, and is deactivated when it is determined the data in the buffer is invalid **(Para [0093])**. Matsumoto suggests that in order to meet increasing demands on channel capacities and for higher speed channels, and improved buffer access method is required **(Para [0007]-[0008])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the buffer access methods taught by Matsumoto in the device taught by AAPA as modified by Uesugi in order to access valid data stored in a buffer by using a read enable signal because the suggestion lies in Matsumoto that this can result in higher speed data transfers.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Uesugi, furthering view of Lassen et al. (US 2002/0087685 A1), hereinafter "Lassen".

Regarding claim 3, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1 wherein the data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)** but does not explicitly recite the limitation of claim 3.

Lassen teaches storing symbols in a temporary storage buffer **(Fig. 3, Decoder Temporary Storage Buffer 255)** prior to decoding. Lassen discloses the temporary storage can be faster access storage such as RAM in which the symbols are accessed from the RAM based on a schedule (i.e. valid data) **(Para [0241])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use RAM as taught by Lassen because the suggestion lies in Lassen that RAM provides faster memory access.

Response to Arguments

Applicant's arguments filed 15 November 2010 have been fully considered but they are not persuasive.

It is examiner's position that AAPA in view of Uesugi fairly discloses the invention of claim 1, and finds the arguments not persuasive. Specifically, given the suggestion in Uesugi that delay can be reduced by demodulating QPSK or 16QAM signals with a 64QAM constellation, and the teaching that one could demodulate 16QAM and QPSK with a 64QAM constellaiton without knowledge of the modulaiton scheme utilised at the transmitter (Para [0074] and [0080]), it would have been obvious to one of ordinary skill in the art to modify the receiver taught by AAPA such that channels could be demodulated prior to analyzing the downlink MAP information using the maximum modulaiton ratio (64QAM). Moreover, given that a 64QAM demappnig process would result in more bits of information (i.e. 6-bits) that actually transmitted for 16 QAM and QPSK (4 and 2 bits repectively), it would have been obvious to one of ordinary skill in

the art that analyzing the downlink MAP as taught by AAPA could be one possible way to determine the number of useful bits of information (i.e. 2, 4 or 6) contained in the bits resulting from the 64QAM demapping process of QPSK, 16QAM or 64QAM symbols. Applicant's arguments also refer to "Walton" as not teaching the claimed limitations. Examiner respectfully submits that no references to "Walton" were made of record or applied as prior art in rejection of the claims. With respect to arguments presented regarding AAPA para 10, examiner cited para 10 and 13 from AAPA to teach the limitation of "reading valid data from the data stored in the slot buffer, based on the analyzed modulation methods for each sub channels and demodulating the valid data, and outputting the demodulated data." The cited portions of AAPA disclose a channel decoder that analyzes the MAP information in order to understand the contents for the demapping process. Since data that has been demapped and stored in the slot buffer (as described by AAPA) cannot be demapped until the decoder analyzes the contents of the MAP message in order to "understand the contents for the QAM demapping process", it is examiner's position that data that is stored in the slot buffer is "valid data". Furthermore, the data that results from the acts of demapping, storing in the slot buffer, and reading (the already valid data) from the slot buffer as described by AAPA result in demodulated data which is then output from the decoder.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joey Bednash whose telephone number is (571)270-7500. The examiner can normally be reached on Mon-Fri 9:00 AM to 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joey Bednash/
Examiner, Art Unit 2461

/Jason E Mattis/
Primary Examiner, Art Unit 2461